Design of low power CMOS inverter using forced nMOS approach

Misbah Saad[1] , Sangeeta Mangesh[2]
Department Of Electronics Engineering, JSS Academy of Technical Education
Noida, India.

Abstract—— This paper introduces a new inverter technique known as reduce swing with forced 2n mos. The proposed (RSFM) reduce swing with forced 2nmos utilizes the property of both reduce swing as well as nmos inverters. Hence it provides low power dissipation as compared to the other inverter techniques. It uses stack method to change the current through mos devices by altering W/L of mos devices. However the penalty for reduction in power is paid by increased delay and layout area.

Index Terms— Delay ,low Power, low swing ,CMOS inverter.

1. INTRODUCTION

In recent years, the demand for low power devices has grown significantly. This growth is mainly due to the fast growth of battery-operated portable devices such as laptop . tablet PC, personal digital assistants, smart phones, and other portable devices. Semiconductor devices are scaled to achieve high-performance and high integration density. Due to increased density of transistors in a die, the power consumption in a die is increasing. Supply voltage is scaled to balance the power consumption within limits. New low-power techniques are required to reduce total power in high-performance nano-scale circuits.

A variety of circuit techniques include transistor sizing, clock gating, multiple and dynamic supply voltage to reduce the dynamic power. For reduction in leakage power, techniques include, dual V_{th}, forward/reverse bias, dynamically varying the V_{th} during run time, sleep transistor and natural stacking.

However, as the feature size shrinks, e.g., to 0.07 and 0.065 μm, static power becomes a great challenge for current and future technologies. According to International Technology Roadmap for Semiconductors (ITRS) [1], [2] Kim concluded that subthreshold leakage power consumption of a chip may exceed dynamic power consumption at the 65-nm feature size. This paper introduces a new inverter technique i.e. reduce swing with forced 2n mos (RSFM) approach for use in low power applications..This technique allows the designer to have low power consumption but at the expense of increased delay and layout area.

The remainder of the paper is as follows: A description of proposed approach in section 2, section 3 describes different types of power dissipation followed by section 4 which briefs different approaches of inverter realization. Section 5 includes simulation and measurement results. The conclusion of the paper is provided in section 6.

2. PROPOSED APPROACH

Reducing power consumption in integrated circuits is of utmost importance for both portable and desktop applications. The power consumed by the clock network, clock trees, buffers, latches and flip-flops, presents a percentage that ranges from 20 to 50% of the total power. Many recent papers have highlighted the issue of how to use a low-swing clock in latches and flip-flops. However these timed circuits are not the only elements to be considered for power consumption.

Reduced swing inverters presented in [3] are used at the node fed by the low-swing sinusoidal clock signal. This is done to reduce the effect of short circuit power. C. Kim. [7] Demonstrated that a low-swing square-wave clock double-edge triggered flip-flop allowed a 78% power savings in the clock distribution network (CDN). Low-swing clocking requires two voltage levels, and these voltage levels can be generated by one of the two schemes: 1) dual-supply voltages and 2) regular power supply. The first technique adds circuit and extra area complexity to the overall chip design and layout. However, it leads to a reduction in the number of clock network transistors which improves power saving [8].

The proposed approach utilizes property of both reduce swing as well as forced nmos inverters. This approach results in a reduced power consumption but with increased delay and layout area. This approach may find applications in low power circuits where low power consumption is of primary concern.

3. DIFFERENT TYPES OF POWER DISSIPATION.

Two types of power dissipation that take place are:

1. Static power dissipation
2. Dynamic power dissipation.

Static power dissipation happens due to the leakage current and leakage current occur due to the off transistor because some minutely current flow in off transistor whether it is pmos or nmos [10].

Dynamic power dissipation occurs due to the charging and discharging of capacitor.

$$P = ACV^2F \quad (1)$$

P is the power consumption, A is the activity factor, C is the switched capacitance, V is the supply voltage, and F is the clock frequency [9].

4. DIFFERENT APPROACHES OF INVERTER REALIZATION

a) CMOS Approach

A CMOS inverter is composed of a pmos device and an nmos device. Its operation can be understood with a simple switch model of the MOS transistor, the transistor is nothing more than a switch with an infinite off resistance (for $|V_{GS}| < |V_T|$), and a finite on-resistance (for $|V_{GS}| > |V_T|$). When input is logic 0, logic 1 is obtained at the output and when input is logic 1, logic 0 is observed at the output. Fig.1 shows the conventional CMOS approach.

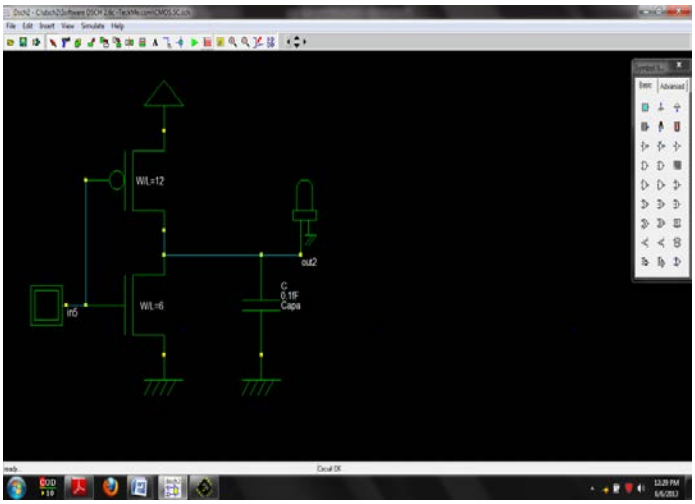

Fig.1. CMOS

b) Stack Approach

Another scheme for reducing leakage power is the stack approach, which uses a stack effect by breaking an existing transistor into two half size transistors to take advantage of the stack effect [4].

It is based on the principle that a pmos and nmos device can be replaced by two equal nmos and pmos devices of half W/L.

Gate terminals of both nmos as well as pmos transistors are tied together and connected to a single source which serves as input for the inverter. Output is taken across a capacitor which serves as a load for the inverter circuit.

However, divided transistors increase delay and could limit the usefulness of this approach.Fig.2 show the stack technique.

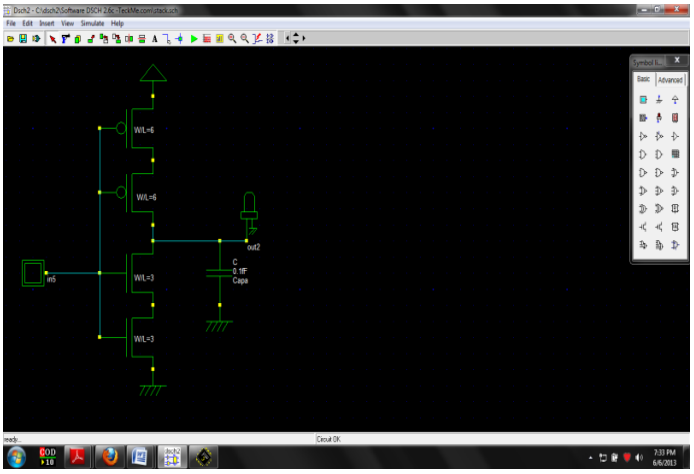

Fig.2. Stack Technique.

c) Reduce swing approach

This is same as conventional CMOS but with an extra pmos at the top whose drain and gate are shorted together. Since $V_{gs}=V_{ds}$,the load pmos device in the reduced swing inverter is always in saturation.. It reduces the voltage at the source of the second pmos in each inverter to approximately V_{dd}-V_{tp} thus turning it off when the low-swing clock signal reaches its peak voltage [5]. Output voltage swings from 0 to V_{dd}-V_{tp} . Pmos acts as a load hence reduces voltage swing to V_{dd}-V_{tp}. This reduction in swing results in a reduced power consumption.Fig.3 shows reduce swing technique.

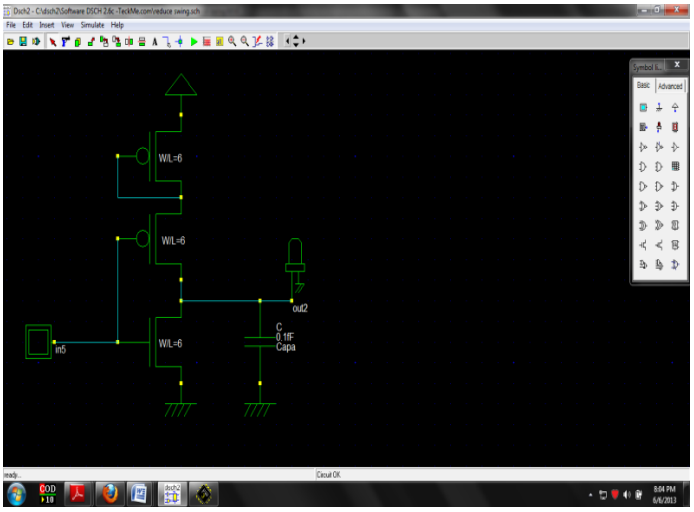

Fig.3. Reduce Swing Technique

d) Forced nmos approach

This approach is same as conventional CMOS but with an added nmos at the bottom. The two nmos devices increase the delay which results in reduction in leakage power in the circuit.

An extra nmos decreases the I_{dd} through mos device hence decreasing power consumption as compared to the conventional CMOS.Fig.4 shows nmos technique.

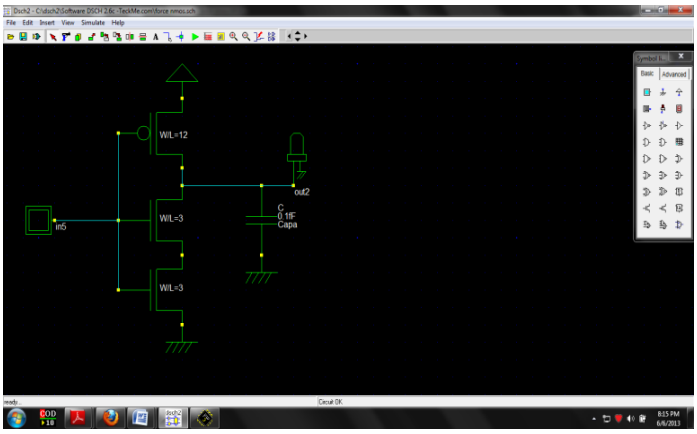

Fig.4. Forced nmos Technique

e) Forced pmos

This is same as conventional CMOS but with an added pmos at the top. Here the addition of two pmos devices increases the delay which results in reduction in leakage power in the circuit.Fig.5 shows forced nmos technique.

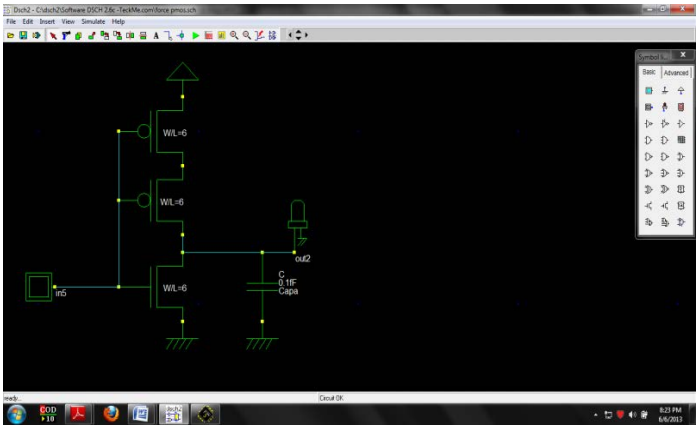

Fig.5. Forced pmos Technique

f) Reduce swing with forced 2nmos(RSFM)

This approach combine's property of both reduce swing as well forced nmos inverters. The load pmos transistor in the reduced swing inverter is always in saturation since $V_{gs}=V_{ds}$. It reduces the voltage at the source of the second pmos in each inverter to approximately $V_{dd}-V_{tp}$ thus switching it off when the low-swing clock signal reaches its peak voltage. This approach has low power consumption but with increased delay and layout area. The output voltage swings from 0 to $V_{dd}-V_{tp}$ .Pmos acts as a load hence reduces voltage swing to $V_{dd}-V_{tp}$. This reduction in swing results in a reduced power consumption. Fig. 6 shows proposed Reduce Swing with forced 2nmos (RSFM).

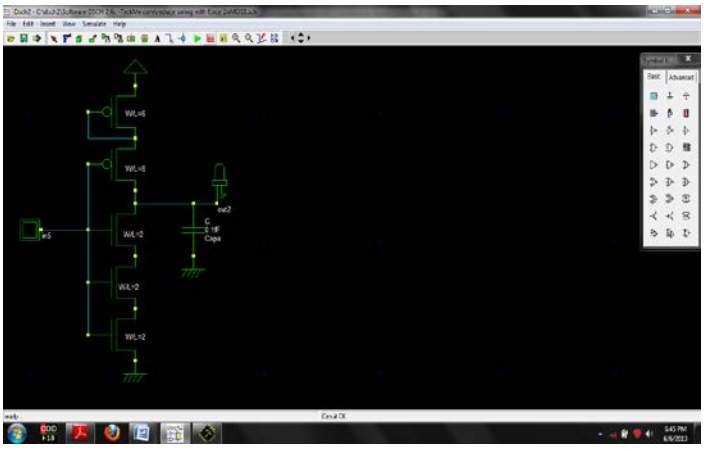

Fig.6. Reduce Swing with force 2nmos(RSFM)

5. SIMULATION RESULTS

The layout and simulation have been performed on Microwind and DSCH.First the schematics are drawn using DSCH.Then a Verilog file is generated in DSCH which is then compiled in Microwind tool to generate the layout and to estimate layout area.0.12µm Technology is used. Simulations are done using level 1 Model.

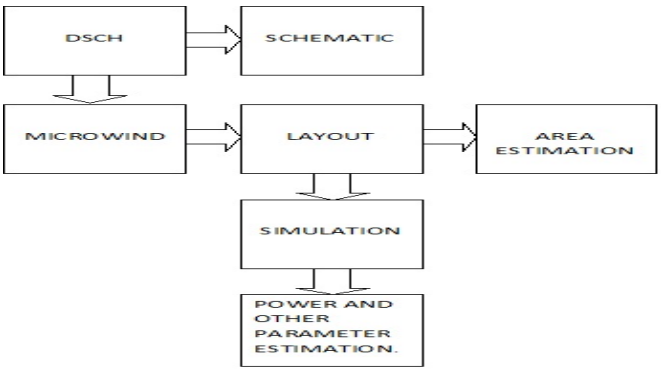

Fig..7. Flow Graph for Layout Area and other parameter estimation

The simulation results for Power Dissipation, Layout Area, Rise Delay, Fall Delay and current is shown in Table 1.Figure 7 shows how microwind and DSCH are used to generate the layout and estimate area and other parameters.W/L of mos devices are kept such that $(W/L)_P=2(W/L)_n$for a symmetric inverter.In this case ,$(W/L)_n=6$ and $(W/L)_{P=}12$. A 0.1fF capacitor is used at the output as a load. This capacitor reduces glitch at the output. Rise delay and fall delay can be observed at the output. Output has been observed for 5ns time duration. Different values of power and current can be observed for different time duration. All simulations have been performed using 0.12µm technology.

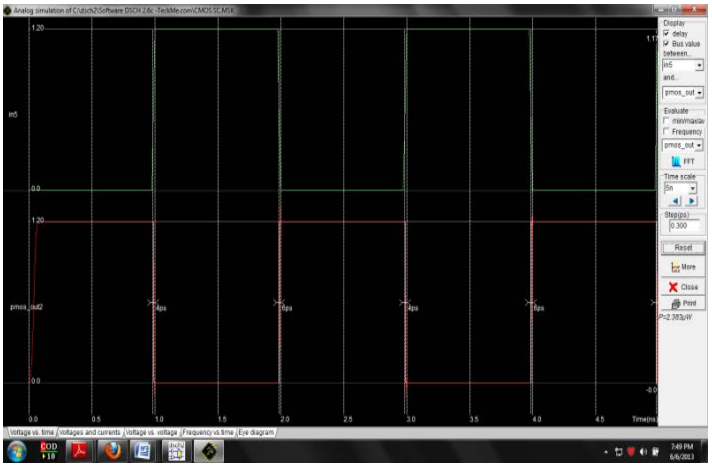

Fig.8(a). CMOS

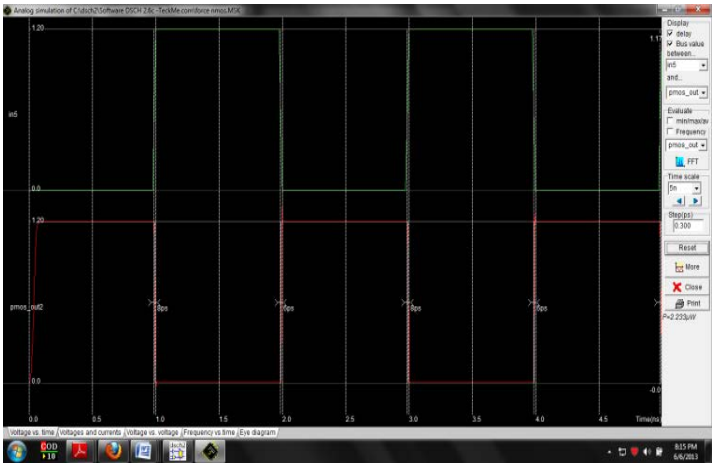

Fig.8(d). Forced nmos

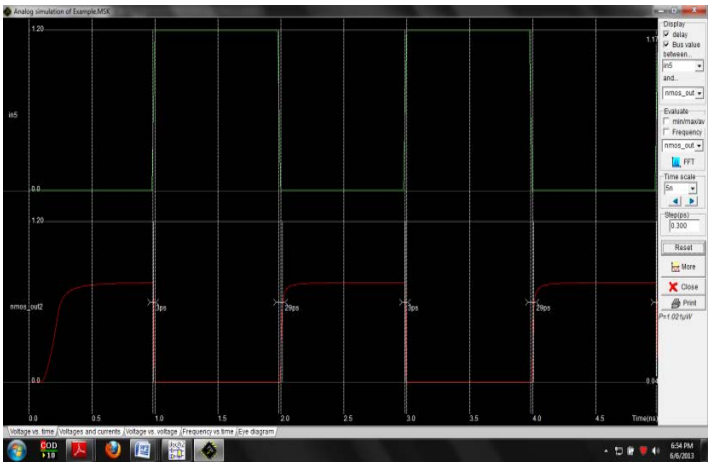

Fig.8(b). Reduce Swing

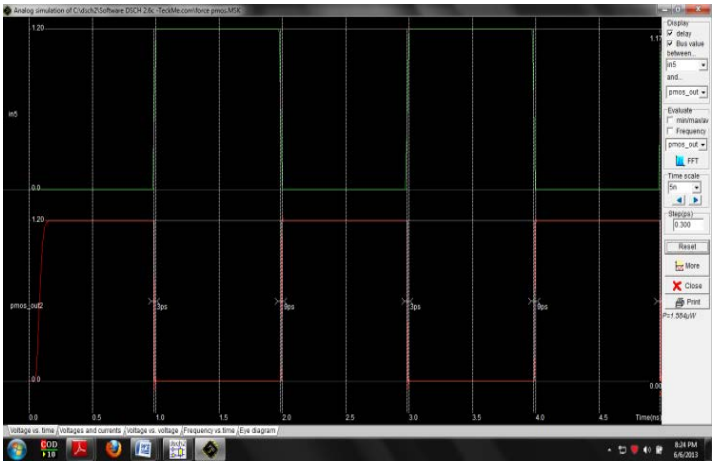

Fig .8(e). Forced pmos

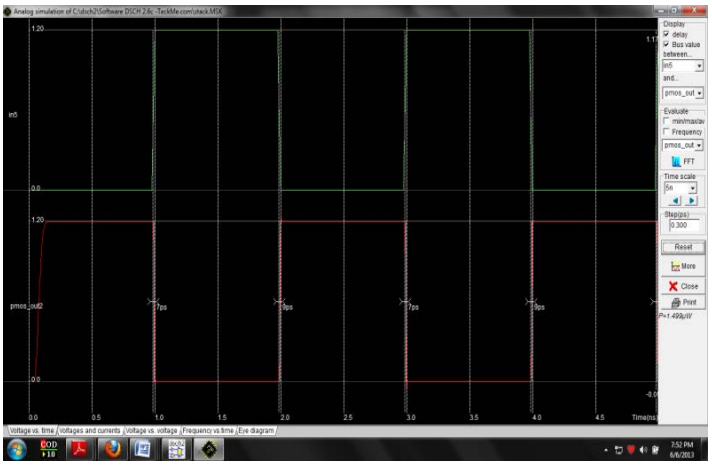

Fig.8(c). Stack

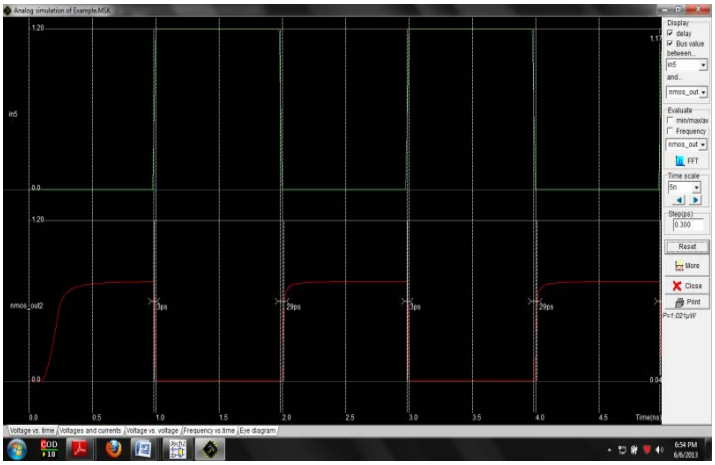

Fig.8(f). Proposed RSFM

Fig.8. Measurement of Rise Delay, Fall Delay and Power Consumption for various approaches of inverter realization.

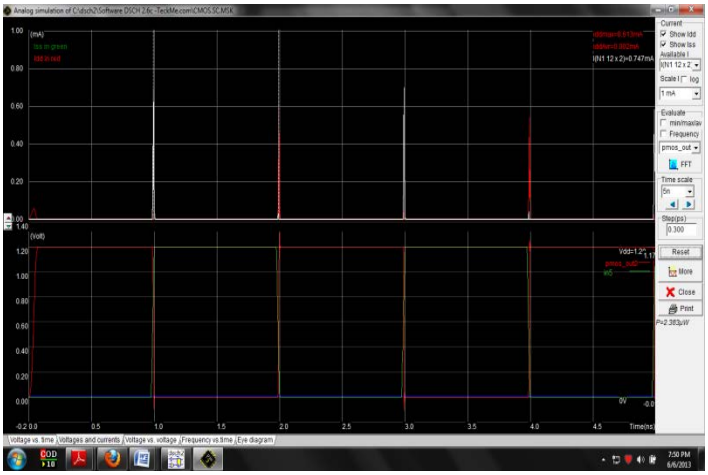

Fig.9 (a). CMOS

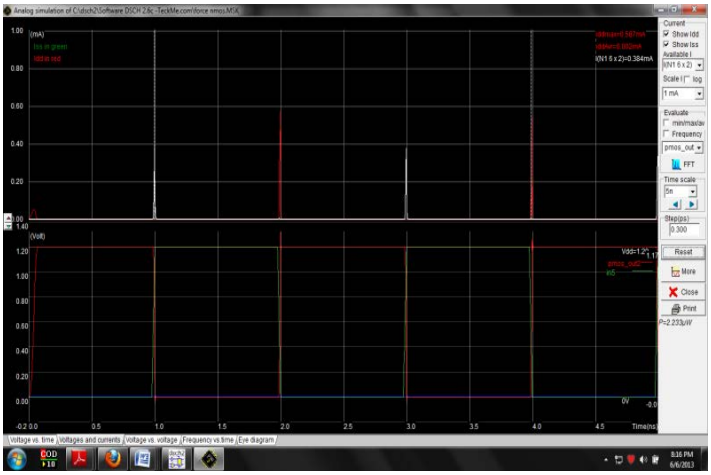

Fig.9(d). Forced nmos

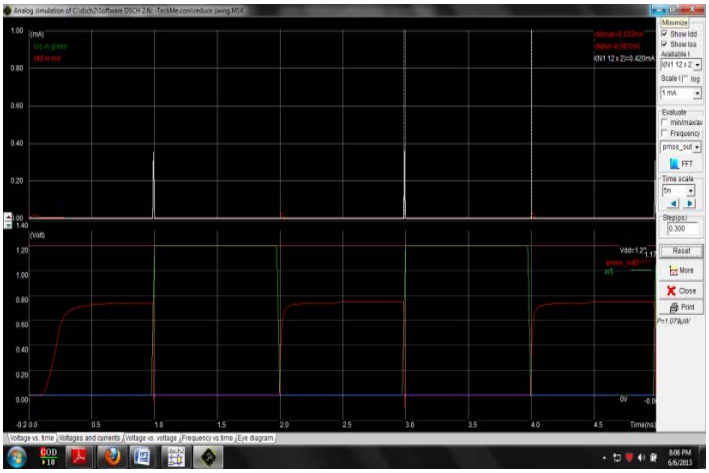

Fig.9(b). Reduce swing

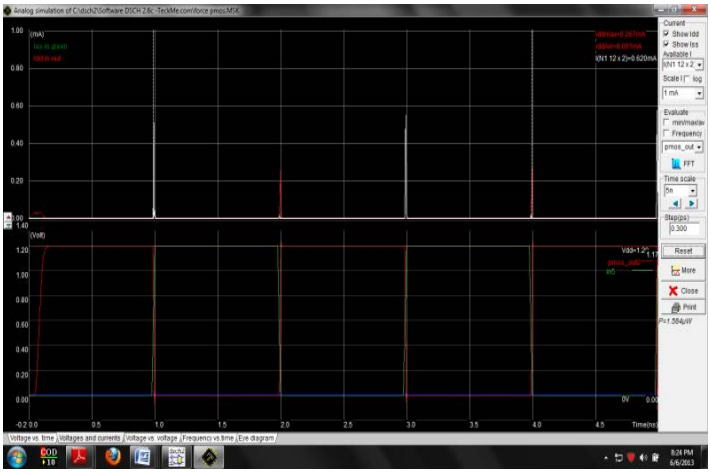

Fig.9(e). Forced pmos

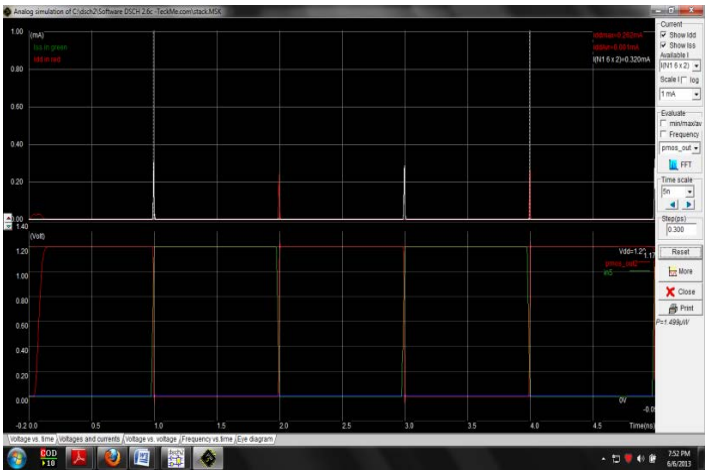

Fig.9(c). Stack

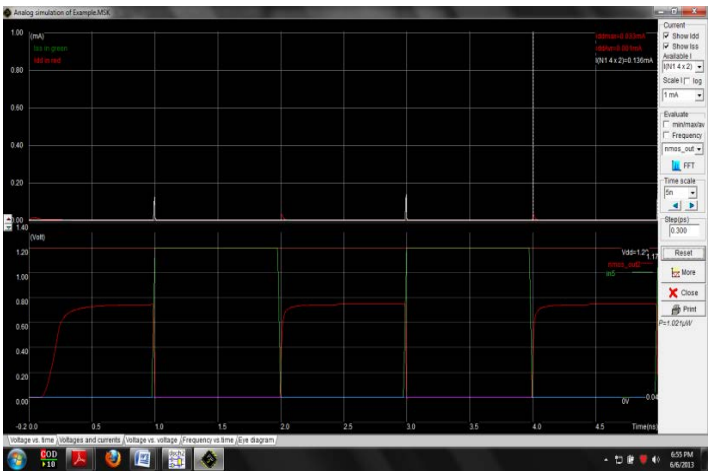

Fig.9(f). Proposed RSFM

Fig.9. Measurement of I_{dd} and I_{avg} for different approaches of inverter realization.

Table .1. Power and other parameter comparison for different inverter realization techniques.

	Rise Delay(ps)	Fall delay(ps)	Power(µw)	$I_{dd\ max}$(mA)	$I_{dd\ avg}$(mA)	Layout Area(µm²)
CMOS	6	4	2.383	0.613	0.002	27.90
Reduce Swing	31	1	1.079	0.033	0.001	27.20
Stack	9	7	1.499	0.262	0.001	37.80
Forced nmos	6	8	2.233	0.587	0.002	37.80
Forced pmos	9	3	1.584	0.267	0.001	29.8
Reduced swing with forced 2n mos(RSFM)	29	3	1.021	0.033	0.001	49.7

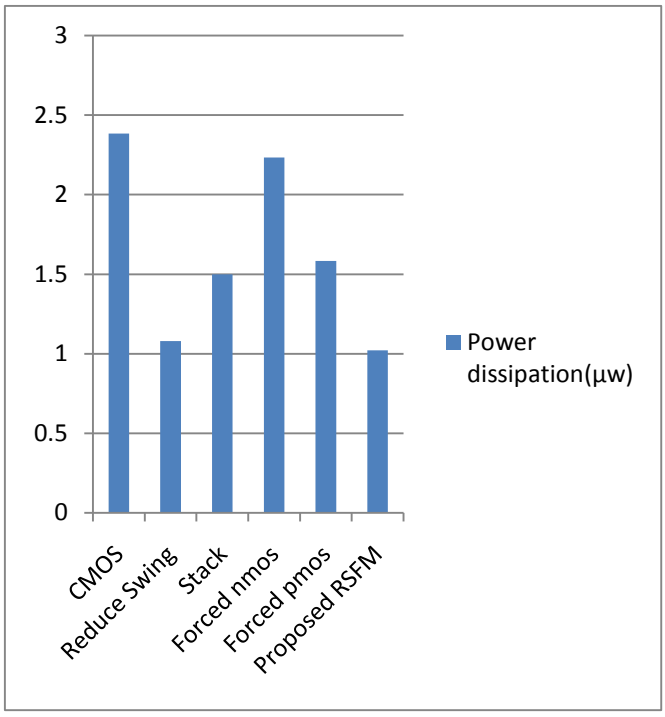

Fig.10. Power dissipation graph for various approaches of inverter realization.

6. CONCLUSION:

This paper proposes a new approach of inverter realization using reduced swing and forced nmos approach. Power consumption is least in the case of Proposed RSFM but with an increased delay and layout area. The Proposed circuits were designed in 0.12µm technology in Microwind and DSCH.

Reduced Power consumption takes place due to reduced W/L of mos circuits as well as reduction in supply voltage.Futher improvements can be done by exploring techniques to reduce delay which is a drawback in the case of proposed RSFM.

REFERENCES:

1)"International Technology Roadmap for Semiconductors," Semiconductor Industry Association, 2005.

2)Se Hun Kim, Vincent J. Mooney III "*Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design"*,IEEE VLSI., 10.1109/VLSISOC.2006.313263 ;pp367-372.

3)J. Pangjun and S. S. Sapatnekar, "Low-power clock distribution using multiple voltages and reduced swings," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 3, , Jun. 2002, pp. 309–318.

4)Kim, N.S. *et al*., 2003. Leakage current: Moore's law meets static power. IEEE Computer,36: pp 68-75.

5) *Seyed* Ebrahim *Esmaeili*, *Asim J. Al-Khalili*, *Glenn E. R. Cowan*: *Low-Swing Differential Conditional Capturing Flip-Flop* for *LC Resonant Clock Distribution Networks*. IEEE Trans. VLSI Syst. 20(8): 1547-1551 (2012),pp 1547-1551

6)Roy, K., S. Mukhopadhaya and H. Mahmoodi Meimand, 2003. Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOS circuits. Proc. IEEE, 91: pp 305-327.

7)C. Kim and S. M. Kang, "A low-swing clock double-edge triggered flip-flop," in *Proc. Symp. VLSI Circuits*, 2001, pp. 183–186.

8) F. H. A. Asgari and M. Sachdev, "A low-power reduced swing global clocking methodology," *IEEE Trans. Very Large Scale Integr. (VLSI)Syst.*, vol. 12, no. 5, May 2004, pp. 538–545,.

9) Rabaey, Pedram "Low power design methodologies", Kluwer Academ-ic, 1997

10) Douglas A.Pucknell,Kamran Eshragian
Basic VLSI Design
Prentice Hall of India.